

D2-CTRINT

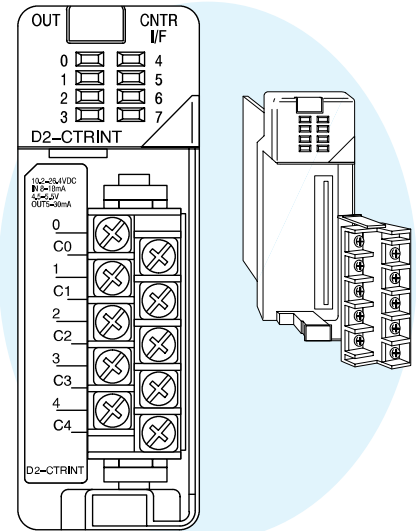
A DL205 CPU, in combination with the D2-CTRINT, provides an incredible diversity of motion and high-speed machine control features. The DL205 CPUs can be configured to work with the D2-CTRINT to provide the following features. You can only use one D2-CTRINT in a DL205 base!

- Up to 2 built-in 5KHz high-speed counters with 24 presets each. When the preset is reached, an interrupt routine in the CPU is executed. The D2-240 and D2-250 support 2 channels and the D2-230 supports 1 channel.
- Quadrature encoder input for clockwise and counter clockwise position control (D2-240/250)
- Programmable pulse output with external interrupts and separate acceleration and deceleration profiles for positioning and velocity control (5K pulses per second max) (D2-240/250)
- 4 External interrupt inputs for immediate responses to tasks.
- Pulse catch feature allows the CPU to read 4 inputs, each having a pulse width as small as 0.1ms.
- Programmable filters for reading up to 4 input signals to ensure input signal integrity
- Combine features to utilize the full potential of the module. Some modes do not use all available points. So in some cases, you can assign one of the other features to the point(s) not used by the main mode of operation.
- Even though some modes can be used together, you cannot use the module for closed-loop control (i.e., you cannot use pulse output and counter input features together).

Overall module specifications	
Module Type	Discrete
Modules per CPU	One, only in slot adjacent to CPU
I/O Points Used	8 inputs, 8 outputs
Field Wiring Connector	Standard 8 pt. removable terminal block
Internal Power Consumption	50mA from 5VDC max., (supplied by the CPU base power supply)
Operating Environment	32°F to 140°F (0°C to 60°C) humidity (non-condensing) 5% to 95%
Manufacturer	Koyo Electronics

Input specifications	
Input	4 pts. sink/source 5KHz Max
Minimum pulse width	100 μSec
Input voltage range	12 or 24VDC ±15%
Maximum voltage	30VDC
Rated input current	10mA Typical 13mA Maximum
Minimum ON voltage	8.0VDC
Maximum OFF voltage	1.0VDC
Minimum ON Current	8.0mA
Maximum OFF Current	1.0mA
OFF to ON response	Less than 30μS
ON to OFF response	Less than 30μS

Output specifications	
Output	2 pts., current sinking, 5KHz Max
Voltage range	5.0VDC±15%
Maximum voltage	5.5VDC
Maximum load current	30mA
Minimum load voltage	4.5VDC
Leakage current	Less than 0.1mA at 5.5VDC
Inrush current	0.5A (10mS)
OFF to ON response	Less than 30μS
On to OFF response	Less than 30μS
External power supply	5.0VDC±10%



Counter Interface Mode 10

Mode 10: two high-speed up counter inputs

Each DL205 CPU has internal features embedded that support high-speed counting up to 5KHz. (Two counters for the D2-240 and D2-250, only one for the D2-230). You connect the external pulse input and reset input signals to the internal counter by using the counter interface module (D2-CTRINT). The embedded counters are independent of the CPU ladder logic execution, so counting is not affected by the scan time. When the counter reaches a

preset value (up to 24 presets per counter), the CPU stops executing the main program and executes an interrupt subroutine that is associated with the UP counter (one interrupt subroutine per UP counter). You can program the subroutine with any of the instructions that are normally available in subroutines. Also, an internal "Equal" relay assigned to each preset is set ON when the associated preset matches the actual count (24 "Equal" relays per counter). This allows you to easily trigger actions based on the current count. For example, you could use Immediate I/O instruc-

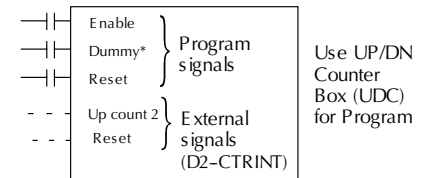
tions to provide a fast response. The CPU resumes normal operations from where it left off after the interrupt subroutine is finished.

Turning the enable of the counter off and on will halt and resume the counting. Counters can reset either by an external signal (X2, X3) or by special internal relays that can be activated by the program. Presets can be either absolute or incremental. Absolute presets are compared directly to the actual count. Incremental presets compare the actual count to the result of adding the associated preset value to the previous preset value.

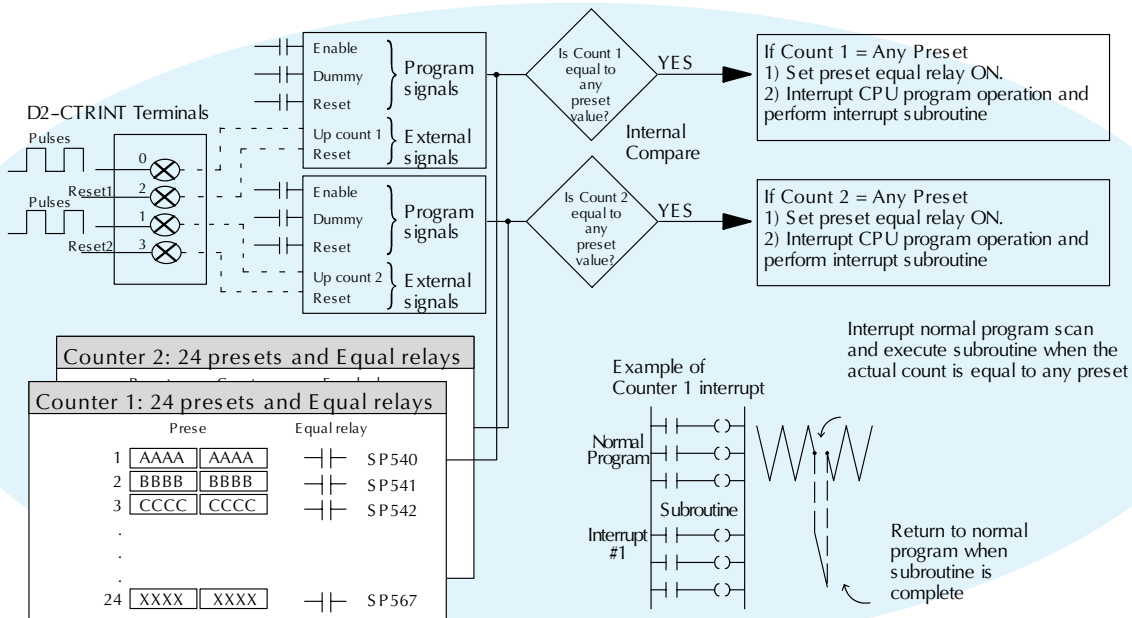
Input Specifications	
Input voltage	12 or 24VDC
Frequency	5KHz maximum
Minimum pulse width	100µs
Maximum count	99,999,999
Preset types	Absolute or Incremental
Number of presets	24 per counter
Interrupt priority	Counter 1 over Counter 2

Input Assignments for Up counter	
Input 1	Up count of UP counter 1 (X0)
Input 2	Up count of UP counter 2 (X1)
Input 3	External Counter 1 reset (X2)
Input 4	External Counter 2 reset (X3)

Built-in High-Speed Counter



Example with two counters



Mode 20: one up/down counter (quadrature counter)

By selecting Mode 20, the two high-speed UP counters (5KHz) embedded internally in the D2-240 and D2-250 CPUs are configured to operate as a single 5KHz Up/Down counter (not available in D2-230). Two external pulse inputs (count up and count down) and one reset input signal are connected to this internal Up/Down counter by means of the D2-CTRINT counter interface module. In addition, there are 2 signals used in the control

program: a counter enable input, and a counter reset input.

Just like the UP counter, the UP/DOWN counter is also independent of the CPU ladder logic execution, so counting is not affected by the scan time. When the counter reaches a preset value (up to 24 presets), the CPU stops executing the main program and executes an interrupt subroutine that is associated with the counter. You can program the subroutine with any of the instructions that are normally available in subroutines. Also, an internal "Equal" relay assigned to each preset is set ON when the associated preset matches the actual count. This

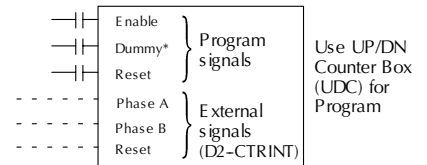
allows you to easily trigger actions based on the current count. For example, you could use Immediate I/O instructions to provide a fast response. The CPU resumes normal operations from where it left off after the interrupt subroutine is finished.

Turning the enable of the counter off and on will halt and resume the counting. Presets can be either absolute or incremental. Absolute presets are compared directly to the actual count. Incremental presets compare the actual count to the result of adding the associated preset value with the previous preset value.

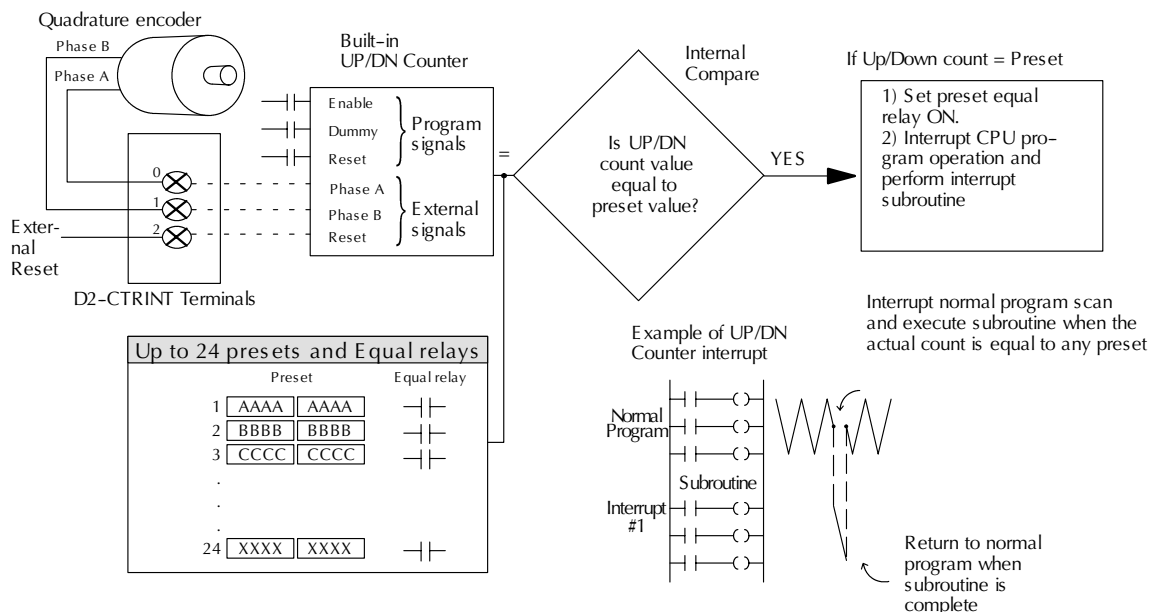
Up/Down Counter Specifications	
Input voltage	12 or 24 VDC
Frequency	5KHz maximum
Minimum pulse width	100µs
Count Range	-8,388,608 to 8,388,607
Preset Types	Absolute or incremental
Number of presets	24 (Two words per preset)

Input Assignment for the Up/Down Counter	
Input 1	Phase A (X0)
Input 2	Phase B (X1)
Input 3	External counter reset (X2)

Built-in UP/DN Counter



Example of Up/Down Counter



Mode 40: four external interrupts

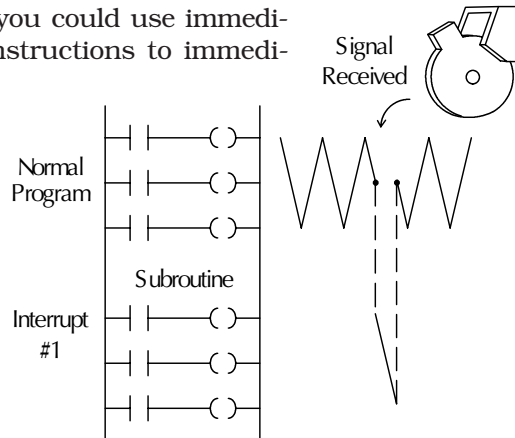
By selecting Mode 40, you can use the Counter Interface as a high-speed interrupt input module. The D2-230\240\250 CPUs support this mode.

An interrupt input is especially useful in applications that have a high priority event which requires special operations to be performed. When this high-priority event occurs, the interrupt

module senses an ON input signal. The module automatically informs the CPU to interrupt its present operation. The CPU immediately suspends its routine scan cycle execution and jumps to a subroutine identified with that particular interrupt input signal point. You can program the subroutine with any of the instructions that are normally available in subroutines. For example, you could use immediate I/O instructions to immedi-

ately read inputs and update outputs without waiting on the normal I/O update cycle. When the subroutine is complete, the CPU automatically resumes the normal scan cycle starting at the exact location from where it was interrupted. The CPU continues the routine scan until another interrupt signal is sensed.

Interrupt Input Specifications	
Point assignments	Four Interrupts (X0, X1, X2, X3)
Minimum pulse width	100µS
Trigger	Leading edge
Interrupt priority	X0 first, X1 second, X2 third, X3 fourth
Interrupt subroutines	Four (INT0, INT1, INT2, INT3)



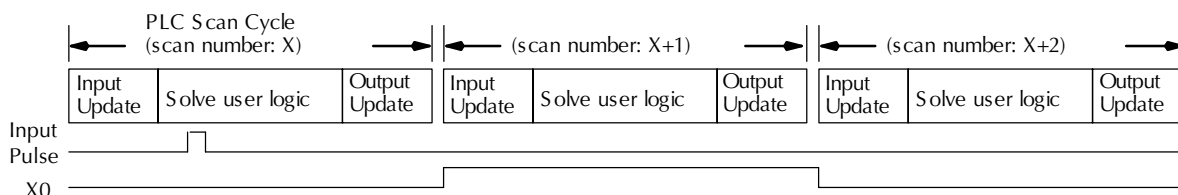
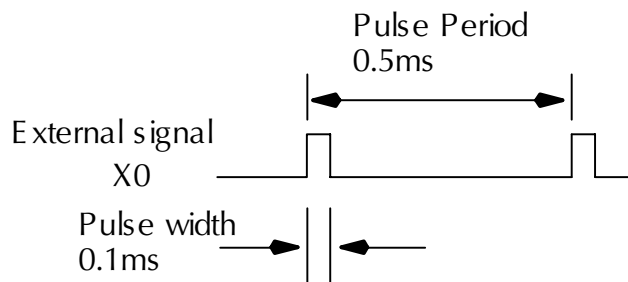
Mode 50: four pulse catch inputs

By selecting Mode 50, the D2-230, D2-240, and D2-250 CPUs can capture very fast (narrow) pulse inputs that cannot normally be detected during the normal input

update cycle. Up to 4 different external inputs (X0, X1, X2, X3), with pulse widths as small as 0.1ms (and a pulse period greater than 0.5ms) can be trapped. When an external pulse is encountered, X0-X3 is set in the ON state for the next scan of the

CPU and automatically set to the OFF state. Like the other modes, the pulse catch feature operates independently of the CPU scan.

Pulse catch input specifications	
Point assignments	Four inputs (X0, X1, X2, X3)
Minimum pulse width	0.1ms
Pulse Period	More than 0.5ms
Trigger	Leading edge



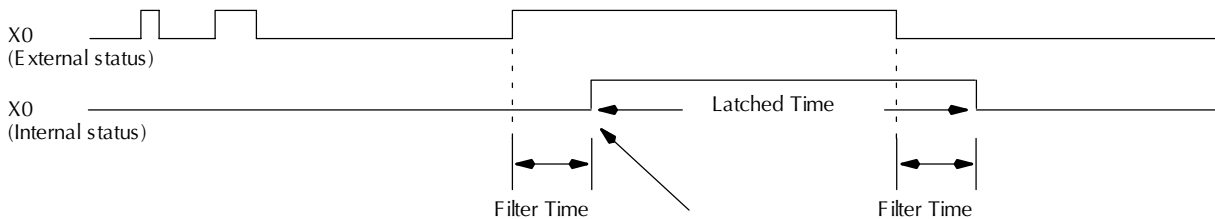
Counter Interface Mode 60

Mode 60: four discrete inputs with filter

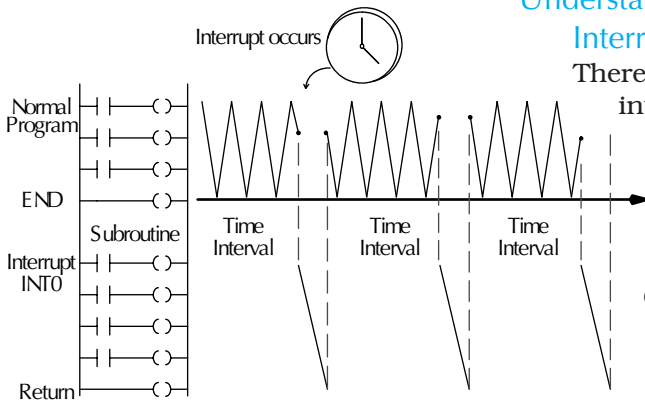
With Mode 60 selected, the D2-230, D2-240, and D2-250 CPUs provide filtering for up to four input signals from the Counter Interface. The filtering helps reduce the possibility of false ON conditions triggering the

program logic. When an external signal is first detected (ON state), a programmable filter is activated which begins a timed countdown. The slight delay temporarily prevents the CPU from reading the input during the normal input update portion of the scan cycle. The ON signal must stay present long enough for the filter to time out. If the ON signal stays present

during the entire filter time, it is latched by the filter and allowed to be accepted by the CPU during the CPU's normal input update portion of the scan cycle. The signal is latched for the remaining duration of the ON signal plus an amount of time equal to the filter time. The filter time can be programmed from 0 to 99ms in 1ms increments.



After the filter delay time, the input is accepted by the CPU.



Understanding the Timed Interrupt

There is also a timed interrupt feature available in our D2-240 and D2-250 CPUs. You do not have to purchase the Counter Interface module to use the timed interrupt. This cyclical inter-

ruption allows you to easily program a time-based interrupt that occurs on a scheduled basis. The CPU's timed interrupt operates in a similar manner to the external interrupt input, but instead of the interrupt subrountine being triggered by an external event, it is now triggered by a cyclical interval of time. This interval can be programmed from 3ms to 999ms. Whenever the programmed time elapses, the CPU immediately suspends its routine scan cycle and jumps to interrupt subrountine INT 0. As with the other modes, when the subrountine execution is complete, the CPU automatically resumes its routine scan cycle starting at the exact location from where it was interrupted. Since the CPU scan time and the interrupt time interval are different, the program gets interrupted at various points in the execution over time. The CPU returns to the point where it left to resume the program execution. If you do choose to use a timed interrupt and the Counter Interface module, you can do so, but you cannot use X0 on the Counter Interface. If you're using the timed interrupt and a normal discrete module, then there are no restrictions.

Counter interface input assignments for timed interrupt mode

X0	Not available for use
X1	Filtered Input, Interrupt, or Pulse Catch
X2	Filtered Input, Interrupt, or Pulse Catch
X3	Filtered Input, Interrupt, or Pulse Catch

Timed interrupt specifications

Timed interrupts	One (internal to CPU)
Time interval	3 to 999ms (1 ms increments)
Interrupt Subrountine	INT0

ruption allows you to easily program a time-based interrupt that occurs on a scheduled basis. The CPU's timed interrupt operates in a similar manner to the external interrupt input, but instead of the interrupt subrountine being triggered by an external event, it is now triggered by a cyclical interval of time. This interval can be programmed from 3ms to 999ms. Whenever the programmed time elapses, the CPU immediately suspends its routine scan cycle and jumps to interrupt subrountine INT 0. As with the other modes, when the subrountine